LISTING OF CLAIMS:

The following listing of claims replaces all previous claims and listings of claims in this application.

Claims 1-9 (Canceled)

10. (Original) A multi-clocked routing chip for use in an emulation system, the multi-clocked routing chip comprising:

a reconfigurable static routing circuit;

a first set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the first set of input/output circuitry is clocked by a first clock signal; and

a second set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the second set of input/output circuitry is clocked by a second clock signal different than the first clock signal.

11. (Presently Amended) The multi-clocked routing chip of claim 10, wherein the first and second sets of input/output circuitry each includes a plurality of one-to-n demultiplexers and a plurality of n-to-one multiplexers, where n is an integer greater than 1.

12. (Presently Amended) The multi-clocked routing chip of claim 10, further comprising a third set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the third set of input/output circuitry is clocked by a third clock signal different than the first and second clock signals.

Claims 13-16 (Canceled)

17. (Original) A system comprising:

a first chip;

a second chip; and

a bi-directional data transfer connection, situated between the first chip and the second chip, providing simultaneous bi-directional data transfer between the first and second chips via a single wire or trace.

18. (Original) The system of claim 17, wherein the first chip includes a detection logic for determining a signal value asserted by the second chip based at least in part on a voltage level of the bi-directional data transfer connection.

19. (Original) The system of claim 18, wherein the detection logic is also for determining the signal value asserted by the second chip based at least in part on a signal value asserted by the first chip.

20. (Original) The system of claim 17, wherein the system comprises an emulator and the first chip comprises a first reconfigurable logic device of a plurality of reconfigurable logic devices.

21. (Original) The system of claim 20, wherein the second chip comprises a first interconnect device of a plurality of interconnect devices interconnecting the plurality of reconfigurable logic devices.

22. (Original) The system of claim 20, wherein the second chip comprises a second reconfigurable logic device of the plurality of reconfigurable logic devices.

23. (Newly Presented) The multi-clocked routing chip of claim 10, wherein signals can be transferred out of the reconfigurable static routing circuit asynchronously to input of signals to the reconfigurable static routing circuit.